**Jiyuan Zhang** Last Update: May 8, 2024

## Personal Information

jiyuanz3@illinois.edu
https://jiyuan.is

## Education

**University of Illinois Urbana-Champaign** Urbana, IL
M.S. in Computer Science Aug 2022 – May 2024
Advisor: Prof. Tianyin Xu
Thesis: A Software Approach to Accelerating Memory Translation for Virtualized Clouds

**New Jersey Institute of Technology** Newark, NJ
B.S. in Computer Science Jan 2020 – May 2022
GPA: 4.0/4.0

## Refereed Conference Publications

1. [**ASPLOS '24**] **Jiyuan Zhang**, Weiwei Jia, Siyuan Chai, Peizhe Liu, Jongyul Kim, and Tianyin Xu. "Direct Memory Translation for Virtualized Clouds". In *Proceedings of the 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Apr 2024. [Link]
2. [**PACT '23**] Weiwei Jia*, **Jiyuan Zhang***, Jianchen Shan, Yiming Du, Xiaoning Ding and Tianyin Xu. "HugeGPT: Storing Guest Page Tables on Host Huge Pages to Accelerate Address Translation". In *Proceedings of the 32nd International Conference on Parallel Architectures and Compilation Techniques (PACT)*, Oct 2023. [Link]
3. [**EuroSys '23**] Weiwei Jia*, **Jiyuan Zhang***, Jianchen Shan, and Xiaoning Ding. "Making Dynamic Page Coalescing Effective on Virtualized Clouds". In *Proceedings of the 18th European Conference on Computer Systems (EuroSys)*, May 2023. [Link]
4. [**ICSE '23**] Wenbo Wang, Tien N. Nguyen, Shaohua Wang, Yi Li, **Jiyuan Zhang**, and Aashish Yadavally. "DeepVD: Toward Class-Separation Features for Neural Network". In *Proceedings of the 45th ACM/IEEE International Conference on Software Engineering (ICSE)*, May 2023. [Link]
5. [**SoCC '22**] Weiwei Jia, **Jiyuan Zhang**, Jianchen Shan, Jing Li, and Xiaoning Ding. "Achieving Low Latency in Public Edges by Hiding Workloads Mutual Interference". In *Proceedings of the 13th Symposium on Cloud Computing (SoCC)*, Nov 2022. [Link]

* Equal contribution authors

## Refereed Journal Publications

1. [**TC '24**] Weiwei Jia*, **Jiyuan Zhang***, Jianchen Shan, and Xiaoning Ding. "Effective Huge Page Strategies for TLB Miss Reduction in Nested Virtualization". To appear in *IEEE Transactions on Computers (TC)*, 2024. [Link]

* Equal contribution authors

## Research Experience

**UIUC xLab**, Prof. Tianyin Xu Aug 2022 – Present

*Direct File Translation for Persistent Memory*

- Working on the design and implementation of a new filesystem that can drastically reduce the file indexing overhead for persistent memory devices.

*Inclusive OS for New Virtual Memory Architectures*

- Working on redesigning the Linux memory management subsystem to provide an inclusive and unified memory management interface for supporting various virtual memory translation schemes.

- Working on implementing and evaluating the new memory system with x86 Radix Page Table and Elastic Cuckoo Hash Page Table.

*Direct Memory Translation for Virtualized Clouds*

- Designed and implemented a novel address translation scheme that minimizes the worst-case memory translation overhead to 1, 2, and 3 for native, virtualized, and nested virtualized memory, with backward compatibility to x86 architecture.
- Evaluated the performance in native, virtualized, and nested virtualized environments with a hardware simulator.

*Using Huge Pages to Accelerate Address Translation for Weak Locality Data*

- Designed and implemented a software system solution to improve the Page Walk Cache efficiency, which strategically clusters page table pages in physical memory.
- Evaluated the effectiveness of such design in a virtualized environment.

**NJIT Operating System Group**, Prof. Xiaoning Ding — Sep 2021 – Aug 2022

*Making Dynamic Page Coalescing Effective on Virtualized Clouds*

- Identified host-guest page size mismatch as a main cause of high TLB misses and low performance in virtualized systems.
- Designed and implemented a software-only solution to page size mismatch in virtualized systems.

*Achieving Low Latency in Public Edges by Hiding Workloads Mutual Interference*

- Designed and implemented a task scheduler that can identify critical paths in workloads and perform adaptive scheduling.
- Evaluated the performance of the task scheduler.

**NJIT SPACE Lab**, Prof. Shaohua Wang — May 2021 – Sep 2021

*Identifying Software Vulnerabilities with Graph-based Neural Networks*

- Designed and implemented an automated toolchain to identify security patches from software repositories, and to extract source code class-separation features.

## Teaching and Mentoring Experience

**Research Mentoring**

- Peizhe Liu (Undergraduate Student, UIUC) — Oct 2023 – Present
  I am mentoring Liu on the project of Direct Memory Translation for Virtualized Clouds.
- Fan Chung (Undergraduate Student, UIUC) — Jan 2023 – Present
  I am mentoring Chung on the project of Inclusive OS for New Virtual Memory Architectures.
- Yiming Du (Junior Student, University of Rhode Island) — Aug 2022 – May 2023
  I mentored Du on the project of Using Huge Pages to Accelerate Address Translation for Weak Locality Data.

**Teaching Assistant**

- UIUC CS 423: Operating Systems Design — Aug 2023 – Dec 2023
  Worked with Prof. Tianyin Xu
- NJIT CS 114: Introduction to Computer Science II — Jan 2021 – May 2021
  Worked with Prof. Calvin M. James

## Professional Experience

**University of Illinois Urbana-Champaign** — Champaign, IL

Graduate Research Assistant — Jan 2024 – Aug 2024

Graduate Research Assistant — Aug 2022 – Aug 2023

**New Jersey Institute of Technology** — Newark, NJ

Undergraduate Research Assistant — Jan 2022 – May 2022

## Awards and Honors

**NJIT President's Medal for Academic Excellence**, NJIT 2022
**Summa Cum Laude**, NJIT 2022
**Dean's List**, NJIT 2020 - 2022

## Talks and Presentations

**Direct Memory Translation for Virtualized Clouds**
- ACM Int'l. Conf. on Architectural Support for Programming Languages and Operating Systems (San Diego, USA), May 1, 2024

**HugeGPT: Storing Guest Page Tables on Host Huge Pages to Accelerate Address Translation**
- Int'l. Conf. on Parallel Architectures and Compilation Techniques (Vienna, Austria), Oct 23, 2023

## Other Projects

**Timing Simulator for Page Walk Latency Analysis**
- Developed a hardware page walker simulator to perform timing simulation for novel virtual memory designs.
- Implemented several state-of-the-art novel designs in the simulator to analyze and compare the performance of these designs.

**Page Table Debugging Framework for Linux Kernel**
- Developed a kernel module to read, modify, and relocate page table entries for the Linux kernel.
- Designed and implemented an interactive page table debugger based on the kernel module to perform page table experiments.

**Automated Configuration Tool for Linux Kernel Compilation**
- Developed an automated kernel compilation configurator to speed up the development process and reduce configuration errors.
- The tool can automatically modify and verify the kernel compilation configuration according to user instructions.

## Grants

Travel grants for EuroSys '23, OSDI '23, and ASPLOS '24

## Services

Artifact Evaluation Committee: SOSP '23